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(54) [Title of the Invention] A METHOD OF MANUFACTURING A THIN FILM TRANSISTOR

(57) [Summary]

[Object] To provide a TFT in which a leak current is reduced without complicated manufacturing steps.

[Structure] Provided is a method of manufacturing a thin film transistor that is a top gate type thin film transistor with a channel containing polycrystalline silicon, in which a thin film transistor that has a source/drain region containing an intrinsic region, a low impurity concentration region, and a high impurity concentration region is formed through two etching steps and one impurity implantation step by the same mask using a gate electrode.

[Scope of Claim for a Patent]

[Claim 1] A method of manufacturing a thin film transistor, characterized by comprising a step of forming a semiconductor layer on an insulating substrate, a step of forming on the semiconductor layer a gate electrode having an extended bottom surface, a step of forming a source/drain region by introducing an impurity into said semiconductor layer with the gate electrode used as a mask, and a step of etching side surfaces of said gate electrode.

[Detailed Description of the Invention]

[0001]

[Field of the Industrial Application] The present invention relates to a method of manufacturing a thin film transistor.

[0002]

[Prior Art] In a display device using a plasma, light emitting diode, liquid crystal, or the like, since a display portion thereof can be made thin, there is increasing a demand for its application to display devices used in an office equipment or a computer, or to special display devices.

[0003] Among those, a liquid crystal display device (TFT-LCD) in which thin film transistors (TFTs) made of amorphous silicon (a-Si) or silicon containing a crystal (polysilicon: poly-Si) are arranged in a matrix as switching elements is high in a display quality with low power consumption, so that a development thereof is being made intensively.

[0004] In particular, the TFT made of the poly-Si has a mobility about 10 to 100 times as high as that of an a-Si TFT and serves as a pixel switching element by utilizing the above advantage. In addition, there has been intensively performed a research and development on a drive circuit integrated type TFT-LCD in which the poly-Si TFT is applied to a peripheral drive circuit to simultaneously form a pixel TFT and a drive circuit TFT on the same substrate.

[0005] While the poly-Si TFT is higher in mobility than the a-Si TFT, it involves a problem in that a leak current (leak current caused to flow at the time of TFT being in an OFF state) is increased as compared with the a-Si TFT. When using it for constructing the drive circuit, this causes particularly no problem, whereas when using it for the pixel switching, this causes a deterioration in an image quality.

[0006] Therefore, there are various types of poly-Si TFT used for a pixel which are devised in structure. When manufacturing a TFT having an offset structure as an example thereof, in order to form a source/drain region and an offset region it is necessary to perform a photolithography step twice. Thus, at least two masks are required for exposure, and exposing steps such as a PEP step are accordingly necessary for each case, with the result that the steps are complicated.

[0007]

[Problems to be solved by the Invention] A conventional manufacturing method for a thin film transistor has a problem in that, although it employs an offset structure advantageous in reducing a leak current, it is necessary to perform an exposing step twice for which at least two masks are required, resulting in complicated steps.

[0008] The present invention has been made in view of the above-mentioned problems and an object thereof is to provide a method of manufacturing a thin film transistor in which the offset structure can be obtained through a single exposing step and therefore manufacturing steps are simplified.

[0009]

[Means for solving the Problem] In order to attain the above-mentioned object, according to the present invention there is provided a method of manufacturing a thin film transistor, characterized by comprising a step of forming a semiconductor layer on an insulating substrate, a step of forming on the semiconductor layer a gate electrode having an extended bottom surface, a step of forming a source/drain region by introducing an impurity into the semiconductor layer with the gate electrode used as a mask, and a step of etching side surfaces of the gate electrode. In this case, although a semiconductor may be a Group-IV semiconductor, or a Group-III-VI compound semiconductor etc., it is preferred to employ silicon since it increases an image quality when being used

for a liquid crystal display device.

[0010]

[Operation] At the time of manufacturing the thin film transistor on a transparent insulating substrate, the etching step of the gate electrode, the impurity implantation step, and the re-etching step are performed using the same mask, so that the manufacturing steps of the offset region in a submicron or micron order can be simplified. Therefore, it is possible to realize a reduction in cost and an increase in yield.

[0011]

[Embodiment] Hereinafter, the present invention will be described in detail based on embodiments thereof as shown in the drawings.

(Embodiment 1) Embodiment 1 will be described with reference to Figs. 1. Figs. 1 show manufacturing steps of an n-channel coplanar type TFT.

[0012] First, on a transparent insulating substrate 101 that is a glass substrate, quartz substrate, or the like, an SiOx film 102 is deposited with a thickness of about 100 nm by a CVD method as a buffer layer. Further, an a-Si:H film is deposited with a thickness of 50 nm by the CVD method, followed by furnace annealing at 450 °C for 1 hour. Thereafter, for example, XeCl excimer laser annealing is performed and thus the a-Si:H film is melted and recrystallized to form a poly-Si film 103. Then, the poly-Si film 103 is subjected to patterning and etching through a

photolithography etc., and is processed into an island shape (Fig. 1(a)).

[0013] Next, an SiOx film 104 is deposited with a thickness of 100 nm by the CVD method as a gate insulating film and then, for example, a phosphor-doped a-Si film 105 is deposited with a thickness of 400nm as a gate electrode (Fig. 1(b)).

[0014] After patterning a resist, photosensitive polyimide 106, or the like through the photolithography, etching is performed to form a gate electrode 107a so as to have an angle $\theta_1 = 25°$ by, for example, a CDE method (Fig. 1(c)).

[0015] Subsequently, without peeling off the resist, polyimide, or the like, phosphor is implanted by an ion implantation method or ion doping method. In the case of the ion implantation method, for example, an accelerating voltage is set to 100 keV and a dosage is set to 5×10^{15} cm^{-2}. Phosphor ions are heavily doped into source/drain regions 108 overlaid with no gate electrode. Thus, obtained are regions which electrically contact the above regions and in which the phosphor ions are implanted through tapered end portions of the gate, i.e., lightly-doped regions 109. In addition, active layer regions adjacent to the lightly-doped regions, which have a film thickness of 215 nm or more and locate directly below the tapered portions, i.e., regions 110 maintained as intrinsic Si are obtained (Fig. 1(d)).

[0016] Next, the resist, polyimide, or the like is not peeled off,

and while being maintained in the same state as it was when used in the etching through the CDE method, it is used as a mask at the time of anisotropic etching through an RIE method. The gate electrode is re-etched at a taper angle θ_2 = 87° by the RIE method to thereby form offset regions 110 of about 600 nm and LDD regions 109 of about 460 nm. Description will be made of the states of the active layer and gate electrode at this time. By re-etching the gate electrode, a length of a gate electrode 107b is reduced, which accordingly makes a channel region slightly shorter. The above-mentioned lightly-doped (LDD) regions 109 and the intrinsic Si regions (offset regions) 110 adjacent to the channel are added to form a portion of the source/drain regions (Fig. 1(e)).

[0017] Thereafter, the resist or the like is peeled off before an interlayer insulating film 111 is deposited with a thickness of about 400 nm by an APCVD method (Fig. 1(f)). Next, for example, the XeCl excimer laser annealing is performed to activate the source/drain regions and the gate electrode 107b. At this time, a laser energy of about 200 mJ/cm^2 is sufficient for the activation thereof. A diffusion length of an impurity is only in the order of 60 nm when a laser activation method is used, so that the offset regions 110 of about 540 nm (0.5 μm) are obtained. Further, the LDD regions 109 and offset regions 110 can be melted at the same time to thereby obtain a proper n/i junction, which contributes to the reduction in the leak current as well (Fig. 1(g)).

[0018] Further, contact holes H are formed by the photolithography (Fig. 1(h)) and, for example, an Al film is formed as source/drain electrodes by a sputtering method, which is then patterned into source/drain electrodes 112 through the photolithography etc., thereby completing the n-channel coplanar type TFT (Fig. 1(i)).

[0019] Here, an additional description is made of a taper processing of the gate electrode 107a, 107b. When etching the gate electrode into a tapered shape, the taper angle of the gate electrode 107a is set to θ_1 degree as shown in Fig. 2. Next, without peeling off the resist etc., while the gate electrode 107a is used as a mask as it is, the impurity is implanted. Further, the resist etc. that has been used when etching the above gate electrode 107a is adopted as the mask and re-etching is performed such that edge portions of the gate electrode 107a are formed at right angles or substantially right angles (θ_2) to form the gate electrode 107b. At this time, it is needless to say that the etching is performed under the condition of $\theta_2 > \theta_1$. A length (L_1) of a region into which the impurity is implanted through the gate electrode 107a and gate insulating film 104 and a length (L_0) of the so-called offset region adjacent to the channel region as the intrinsic polysilicon are controlled according to the film thickness of gate electrode 107a, 107b, an ion accelerating voltage, the angle of the tapered portion of the gate electrode (θ_1, θ_2), and the like. Fig. 3 shows an average impurity density in the active layer 103 in this case. Thus, through

one impurity implantation step, three regions consisting of a high impurity concentration region 108 ($>L_1$), a low impurity concentration region 109 ($L_1>L_0$), and the offset region 110 ($L_0>0$) can be formed based on a distance from the gate electrode end 107b.

[0020] Alternatively, the gate electrode is etched in two steps under the above condition ($\theta_2>\theta_1$) and then is used as the mask to further add the impurity at a low concentration, so that an LDD structure can be also realized.

[0021] At this time, it is preferable in view of a high reliability that a ratio (L_1/L_0) of the length (L_1) of the poly-Si region (offset region) 104 containing no impurity to the length (L_0) of the low impurity concentration region 105 is set to 0.1 or more.

[0022] By using the manufacturing method as described above, an additional mask is unnecessary to form the offset region. Accordingly, this eliminates the additional PEP step or the like which is required therefor, so that the steps can be significantly simplified.

[0023] In the TFT of the present invention, it is possible to readily obtain the offset structure and reduce the leak current to about 7×10^{-11} A, and irrespective of the tapered gate electrode, the phosphor ions are prevented from being implanted into the gate insulating film directly below the above-mentioned gate electrode, with the result that the reliability of the TFT is improved.

(Embodiment 2) This embodiment differs from Embodiment 1 in that

GaAs serving as the compound semiconductor is applied to a semiconductor instead of Si, and a Schottky electrode made of WNx is used for the gate electrode. In this case, the gate insulating film as in Embodiment 1 is unnecessary, so that on an Si substrate a GaAs layer and a gate electrode are formed in the stated order with the gate electrode formed into a tapered shape (trapezoid with the bottom surface extended). Through the gate electrode, impurity is implanted by the ion implantation to form the source/drain regions and then the side surfaces of the gate electrode are etched in the same manner as in Embodiment 1. The GaAs layer below the etched portions serves as offset regions. Thus, although differing from Embodiment 1 in a material system, this embodiment makes it possible to form the coplanar type TFT using the GaAs with the structure provided with the offset region as in Embodiment 1. It is also possible to effect the Exhibit-A as in Embodiment 1.

[0024] Note that, the description of the present invention has been directed to the coplanar type TFT but various modifications thereof are possible without departing from a gist of the present invention. For example, TFTs such as a stagger type TFT in which the gate electrode locates above the source/drain region and the channel region may be embodied as well. Further, needless to say, the present invention can be applied to an n-channel or p-channel TFT. As for a material for the gate electrode, a high melting point metal and its derivative, nitride, or the like can be employed. As for

the gate insulating film, silicon nitride, silicon oxynitride, or the like can be used, and in addition, as for the source/drain region and channel region, various polycrystalline or amorphous semiconductors can be used.

[0025]

[Effects of the Invention] According to the present invention, the photolithography step adapted to form the offset region is eliminated, whereby the manufacturing steps can be simplified. Thus, it is possible to reduce the cost and increase the yield.

[Brief Description of the Drawings]

[Figs. 1] Sectional views showing an embodiment of the present invention in the step order.

[Fig. 2] An enlarged view showing a main part of the embodiment of the present invention.

[Fig. 3] A view illustrating the embodiment of the present invention.

[Description of Reference Numerals]

101 substrate

102 buffer layer

103 polycrystalline silicon channel

104 gate insulating film

107a, 107b gate electrode

108 source/drain region

109 low impurity concentration region

110 offset region

111 interlayer insulating film

FIG. 1

LASER LIGHT

FIG. 3

AVERAGE IMPURITY DENSITY IN ACTIVE LAYER

DISTANCE FROM GATE ELECTRODE END PORTION